UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,557	01/23/2004	You-Yuh Shyr	O2Micro 99.05CON2	7508

32047 7590 08/15/2006

GROSSMAN, TUCKER, PERREAULT & PFLEGER, PLLC
55 SOUTH COMMERICAL STREET
MANCHESTER, NH 03101

EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 08/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,557	SHYR ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-30* is/are rejected.

7)☒ Claim(s) *20-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a non-Final Office Action in response to the present US Application filed 01/23/2004, which is a CON of 10/266,536 filed 10/08/2002, now US Patent No. 6,720,800, and which is a CON of 09/489,660 filed 01/24/2000, now US Patent No. 6,472,897.

Claims 1-16 have been cancelled.

Claims 17-30 are presently under examination and still pending in the Application.

Drawings

The drawings received on 23 January 2004 are acceptable.

Specification

The disclosure is objected to because of the following informalities:

The status of copending application Serial No. 10/266,536 filed October 8, 2002, should bed updated to "now US Patent No. 6,720,800". Appropriate correction is required.

The specification is objected to under 37 CFR 1.71 because the specification lacks an enabling description for claims 17 and 27 in reference to the term "pin released" described in paragraph 28 of the specification.

Claim Objections

Claims 20-26 are objected to because of the following informalities:

Claims 20 and 21 in passim recite: "adapted to ...' It has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138. Appropriate correction is required.

Claims 21 and 24, "said test signal" should be changed to "said varying test signal" to provide antecedent basis for "a varying test signal".

Claim 21, "in response thereto" should be changed to --in response to the trim cell array digital signal--.

Claim 21, "that resulted" should be changed to --that results--

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 17-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 17 and 27 recite the term "pin released" which renders the claims indefinite, because the word "released" or "releasing" fails to clearly define the status of the pin in relation to the action taken by the after package trim circuit. Applicant's specification describes, "releases the register for use by the IC. Additionally, the trim circuitry includes isolation circuitry to release the package pins utilized during testing, so

that the package pins can be used by the IC as intended". Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). Based on the Applicant's specification description above, the term "released" or "releasing" is used by the claim to mean "enable/disable or active/non-active", while the accepted meaning is "free from restraint". The term is indefinite because the specification does not clearly redefine the term.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 17-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (U.S. Patent No. 6,184,720) filed: June 17, 1999; issued: February 6, 2001.

Regarding independent Claims 17, 27, Kim discloses an apparatus and method for an integrated circuit semiconductor device, Figures 2-4, comprising:

An after package trim circuit (internal voltage generating circuit 100).

Pins (TP0, TP1, . . . , TPn) during a first time interval (test mode) utilized by the (internal voltage generating circuit 100) for a first function corresponding to the test mode activated during the test mode signal Ptest in the test mode signal generator 350. The pseudo fuse circuit block 330 is activated in response to the test mode signal Ptest so that it produces the positive output CUT and the negative output CUTB based on the signals applied to the plurality of test power voltage pads TP0, TP1, . . . , TPn.

Pins (TP0, TP1, . . . , TPn) released when the fuse circuit block 340 is activated when the test mode signal Ptest is non-active (or activated except for test mode), so that it produces the positive output CUT and the negative output CUTB in accordance with the programmed state of the fuse, corresponding to the second time interval of the IC for a second function (during the normal mode of operation when Ptest is non-active).

Regarding Claim 18, 28, Kim discloses pins (TP0, TP1, . . . , TPn) test power voltage pads, which receive a common voltage signal (Vext) during the test mode, each of which can be selectively applied with the external power voltage Vext and a ground voltage Vss during test;

Regarding Claim 19, 29, Kim discloses (internal voltage generating circuit 100) includes programmable control signal generator 300 and a voltage level trimming unit 400, which generate a trim voltage signal represented by a trim signal value (S) (control

signals S0, S1, S2, S3, S4, S5, S6, S7 and SB0, SB1, SB2, SB3, SB4, SB5, SB6, SB7), which is added to an initial reference voltage Vr1 generated by the reference voltage generator 200, which generates the reference voltage Vr1 using the external power voltage Vext, which is applied from outside of the semiconductor device. Then the voltage level-trimming unit 400 produces the trimmed reference voltage Vr2, which is a function of Vr1 and the trim signal value (S). The output voltage Vr2 of the voltage level-trimming unit 400 can be controlled by suitably programming (e.g. selectively cutting) the fuses included in the fuse programmable control signal generator 300, as shown in Figures 2, 5-7.

Regarding Claim 20, 30, Kim discloses wherein the (internal voltage generating circuit 100) comprises, an after-package trim cell circuit array (fuse programmable control signal generator 300) as shown in Figures 2 to 4, 6, for providing digital signals (control signals S0, S1, S2, S3, S4, S5, S6, S7 and SB0, SB1, SB2, SB3, SB4, SB5, SB6, SB7) representative of a trim signal.

An output decision circuit (voltage level trimming unit 400) to receive the digital signals and provide an analog voltage reference signal Vr2, where the Vr2 is a combination of trim signal value (S) corresponding to the (control signals S0, S1, S2, S3, S4, S5, S6, S7 and SB0, SB1, SB2, SB3, SB4, SB5, SB6, SB7) and the initial reference voltage Vr1.

The voltage level-trimming unit 400 applies its output Vr2 to the internal voltage driver 500. At this time, the degree of trimming depends on the multiple control signal

S. The internal voltage driver 500 generates the internal power voltage Vint for driving the internal circuit 600, based on the voltage Vr2, Figures 2-4.

Regarding independent Claim 21, Kim discloses an after package trim circuit (internal voltage generating circuit 100), comprising:

An after-package trim cell circuit array (fuse programmable control signal generator 300) as shown in Figures 2 to 4, 6, to receive a varying test signal (TP0, TP1, . . . , TPn) and provide digital signals (S0, S1, S2, S3, S4, S5, S6, S7 and SB0, SB1, SB2, SB3, SB4, SB5, SB6, SB7) representative of a trim signal.

An output decision circuit (voltage level trimming unit 400) to receive the digital signals and provide an analog voltage reference signal Vr2, where the Vr2 is a combination of trim signal value (S) corresponding to the (control signals S0, S1, S2, S3, S4, S5, S6, S7 and SB0, SB1, SB2, SB3, SB4, SB5, SB6, SB7) and the initial reference voltage Vr1.

The voltage level-trimming unit 400 applies its output Vr2 to the internal voltage driver 500. At this time, the degree of trimming depends on the multiple control signal S. The internal voltage driver 500 generates the internal power voltage Vint for driving the internal circuit 600, based on the voltage Vr2, Figures 2-4.

Regarding Claim 22, Kim discloses test signals (TP0, TP1, . . . , TPn) comprises test power voltage pads coupled to the fuse programmable control signal generator 300.

Regarding Claim 23, Kim discloses output decision circuit (voltage level trimming unit 400) comprises a digital to analog circuitry equivalent to an converter (DAC) to receive the trim cell array digital signal (control signals S0, S1, S2, S3, S4, S5, S6, S7

and SB0, SB1, SB2, SB3, SB4, SB5, SB6, SB7) and the initial reference voltage Vr1 and to provide an analog trim current signal representative of said trim cell array digital signal Vr2.

A resistive element (R0-R8) to convert the analog trim current signal into a trim voltage signal, which is then added to an initial voltage reference signal Vr1, with a resulting trimmed reference signal Vr2, as shown in Figure 7, which is a detailed circuit illustrating one example of the voltage level trimming unit shown in Figures 2 to 4.

Regarding Claims 24, 25, 26, Kim discloses a programmable test signal (TP0, TP1, . . . , TPn), which inherently is stored in a register to provide the test signal to the fuse programmable control signal generator 300. The inherent register is isolated from the fuse programmable control signal generator 300 during the test mode signal Ptest generated by the test mode signal generator 350. An isolation trim cell circuit corresponding to the (test mode signal generator 350) for generating the test mode signal Ptest to isolate the inherent register from the fuse programmable control signal generator 300.

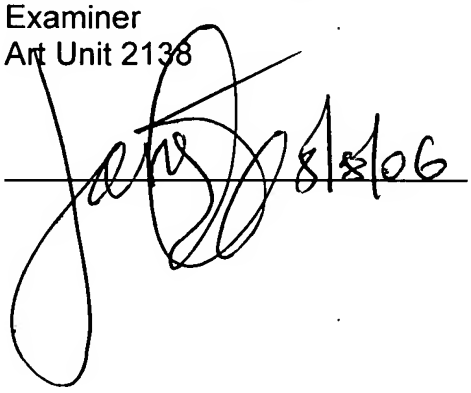
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Examiner
Art Unit 2138



U.S. Patent and Trademark Office
Alexandria, VA 22314
Tel: (571) 272-3824, Fax: (571) 273-3824
james.kerveros@uspto.gov

Date: 8 August 2006
Office Action: Non-Final Rejection